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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/674,317	09/29/2003	Ying-Ren Lin	59970 (71987)	4629

7590 09/22/2005

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EXAMINER	
CARPIO, IVAN HERNAN	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 09/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/674,317	LIN ET AL.	
	Examiner	Art Unit	
	Ivan H. Carpio	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-15 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-15 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 9-29-03 is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 1- 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Mizunashi (US Patent 6528734).

With respect to claim 1 Mizunashi teaches a ground pad structure (Fig. 3) for preventing solder extrusion, comprising: a ground plane (Fig.3, Fig. 3, GP), which is made of a conductive material (Note. If it's a ground plane it must conduct and therefore be made of conductive material) and provided on a substrate of a semiconductor package; and a plurality of ground pads (Fig. 3, elements 2) formed on the ground plane; wherein a part of the ground pads, which are located on the circumference of the ground plane (Fig. 3, pads 2 are located on the circumference of ground plane GP), are non-solder mask defined ground pads (Fig.3, as can be seen no solder mask defines element 2).

With respect to claim 2 and with all the limitations of claim 1, Mizunashi teaches that the non-solder mask defined ground pads disposed on the circumference of the ground plane are protruded from and partially extended (Fig.3, note that ground pads

element 2 are extended from the circumference of GP) from the circumference of the ground plane.

With respect to claim 3 and with all the limitations of claim 2, Mizunashi teaches wherein the ground pads are arranged in a matrix array (Fig. 4a).

With respect to claim 4 and with all the limitations of claim 2, Mizunashi teaches that the ground plane is disposed on a central portion (Fig.3, element GP, Note that the ground plane is on a central position) of the substrate of the semiconductor package.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 5,6,8-10,12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizunashi in view of Hanson (US Patent 5841075).

With respect to claim 5 Mizunashi teaches a semiconductor package (Fig. 3) having a ground pad structure for preventing solder extrusion, comprising: a substrate (Fig.3, element 1), which has an insulative dielectric layer (Fig. 3, element 11), a plurality of conductive traces (Fig. 3, elements SP and VP) disposed above and beneath the dielectric layer, and an insulative layer (Fig. 3, element 21) for covering the conductive traces and the dielectric layer and having a plurality of openings (Fig. 3, element 23), wherein a non-ground pad (Fig. 3, elements 22 and 2, not connected to

ground) is formed on a terminal (Fig.3, elements 23)of each of the conductive traces and exposed from one of the openings; a ground pad structure (Fig. 4a), which has a ground plane (Fig. 3, element GP) made of a conductive material, and a plurality of ground pads (Fig. 3, elements 2) formed on the ground plane, wherein the ground plane is provided on the dielectric layer of the substrate and covered by the insulative layer (Fig. 3, Note GP is between 21 and 11), and the ground pads are exposed from the openings of the insulative layer, and wherein a part of the ground pads, which are disposed on the circumference of the ground plane, are non-solder mask defined ground pads (Fig. 3, note that there is no solder mask defining ground pads 2); a semiconductor chip (Fig. 3, element 3), which has an active surface (Fig. 3, element 3 the bottom surface) and a corresponding inactive surface (Fig. 3, element the top surface), ; an encapsulant body (Fig. 3, element 4, column 5, lines 26-31), which encapsulates the semiconductor chip, the insulative layer, and a portion of the dielectric layer; and a plurality of conductive elements (Fig. 3, elements 6) implanted under the substrate. Mizunashi does not specifically teach that the active surface being formed with a plurality of non-ground conductive metal solder means and ground conductive metal solder means so as to electrically solder the non-ground conductive metal solder means and ground conductive metal solder means of the semiconductor chip to the corresponding non-ground pads and ground pads on the substrate, but does say that the device chip is mounted and connected on the mounting pads by in a flip chip mounting method. It is well known in the art to use solder mounting for flip chip mounting method, Hanson teaches that flip chip mounting (column 1, lines 36-43)

entails solder bumps on a die or chip, flipping the chip over, aligning the chip with the contact pads on a substrate, and reflowing the solder balls in a furnace to establish bonding between the chip and the substrate. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the flip chip mounting method taught by Hanson to mount the semiconductor chip (ground and non-ground pads), taught by Mizunashi, to the substrate because it is well known in the art making manufacture easy and that using this technique the maximum number of I/O and power/ground terminals available can be increased, and signal and power/ground interconnections can be more efficiently routed on the chip (Hanson column 1, lines 46-50).

With respect to claim 6 and with all the limitations of claim 5, Mizunashi teaches that the semiconductor package is a flip-chip (column 5, lines 32-35 and claim 4) semiconductor package.

With respect to claim 8 and with all the limitations of claim 5, Mizunashi teaches the insulative layer (Fig. 3, element 21) is a solder mask layer.

With respect to claim 9 and with all the limitations of claim 5, Mizunashi teaches that the non-solder mask defined ground pads disposed on the circumference of the ground plane are protruded from and partially extended (Fig.3, note that ground pads element 2 are extended from the circumference of GP) from the circumference of the ground plane.

With respect to claim 10 and with all limitations of claim 5, Mizunashi teaches that the non-ground pads are non-solder mask defined (Fig. 3, element 22(24) are not defined by a solder mask) non-ground pads.

With respect to claim 12 and 13 with all the limitations of claim 5, Hanson teaches that the conductive metal solder means are solder balls (column 1, lines 40-41).

With respect to claim 14 and with all the limitations of claim 5, Mizunashi teaches that the non-ground pads and the ground pads are arranged in a matrix array (Fig. 4A).

With respect to claim 15 and with all the limitations of claim 5, Mizunashi teaches that the ground plane (Fig.3, element GP, Note that the ground plane is on a central position) is disposed on a central portion of the substrate.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mizunashi and Hanson in view of Jones (US Patent 5541450).

With respect to claim 7 and with all the limitations in claim 1, Mizunashi teaches all of the limitations but does teach specifically that the dielectric layer is made of an insulative material selected from the group consisting of Bismaleimide Triazine Resin, Polyimide, FR-4 Resin and FR-5 Resin. Jones teaches a dielectric layer made of Bismaleimide Triazine Resin or FR-4 Resin (column 2, lines 17-19). It would have been obvious to make the dielectric layer taught by Mizunashi because since in semiconductor applications it is typically (column 2, lines 17-19) made from Bismaleimide Triazine Resin or FR-4 Resin, manufacturing parts and process would be easy to find and cost effective.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mizunashi and Hanson in view of Beroz (US Patent 6329605).

With respect to claim 11 and with all the limitations of claim 10, Mizunashi teaches all the limitations except that each opening in the insulative layer is being sized larger than the corresponding non-ground pad for exposing the non-ground pad. Beroz teaches an insulating layer (Fig.1, element 230) with openings (Fig. 1, element 232) being sized larger than connecting pads (Fig. 1, element 220a). It would have been obvious to make the openings and ground pads taught by Mizunashi with the relative sizes taught by Beroz because small mistakes in the centering of the pads with the openings would be compensated since the openings are larger than the pads.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. US Patents 6448639 and 6384476 both teach a matrix array ground pad structure for a semiconductor device. US Patent 6504169 discloses a non-solder mask defined ground pads for a semiconductor device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ivan H. Carpio whose telephone number is 571-272-8396. The examiner can normally be reached on M-R 6:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kammie Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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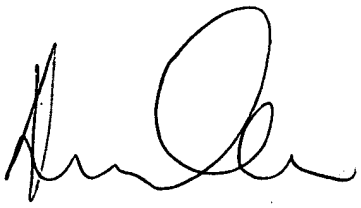

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